

NLX2G00

Dual 2-Input NAND Gate

The NLX2G00 is an advanced high-speed dual 2-input CMOS NAND gate in ultra-small footprint.

The NLX2G00 input structures provide protection when voltages up to 7.0 volts are applied, regardless of the supply voltage.

Features

- High Speed: t_{PD} 2.4 ns (typical) at $V_{CC} = 5.0$ V
- Designed for 1.65 V to 5.5 V V_{CC} Operation
- Low Power Dissipation: $I_{CC} = 1$ μ A (Max) at $T_A = 25^\circ$ C
- 24 mA Balanced Output Sink and Source Capability
- Balanced Propagation Delays
- Overvoltage Tolerant (OVT) Input Pins
- This is a Pb-Free Device

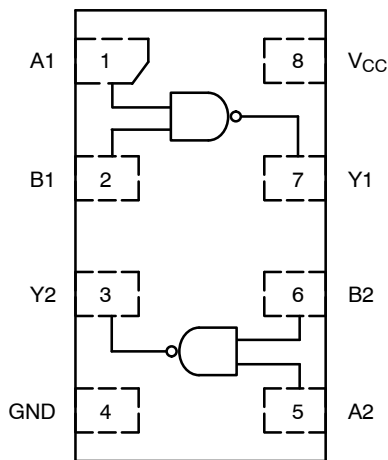


Figure 1. Pinout

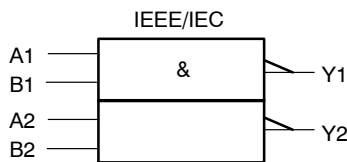


Figure 2. Logic Symbol



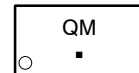
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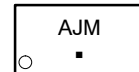
MARKING DIAGRAMS



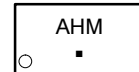
ULLGA8
1.45 x 1.0
CASE 613AA



ULLGA8
1.6 x 1.0
CASE 613AB



ULLGA8
1.95 x 1.0
CASE 613AC



XX = Specific Device Code
M = Date Code
▪ = Pb-Free Package

PIN ASSIGNMENT

Pin	Function
1	A1
2	B1
3	Y2
4	GND
5	A2
6	B2
7	Y1
8	V_{CC}

FUNCTION TABLE

$$Y = \overline{AB}$$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH Logic Level
L = LOW Logic Level

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

NLX2G00

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	-0.5 to +7.0	V
V_{IN}	DC Input Voltage	-0.5 to +7.0	V
V_{OUT}	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current $V_{IN} < GND$	-50	mA
I_{OK}	DC Output Diode Current $V_{OUT} < GND$	-50	mA
I_O	DC Output Source/Sink Current	± 50	mA
I_{CC}	DC Supply Current per Supply Pin	± 100	mA
I_{GND}	DC Ground Current per Ground Pin	± 100	mA
T_{STG}	Storage Temperature Range	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	TBD	°C
T_J	Junction Temperature Under Bias	TBD	°C
θ_{JA}	Thermal Resistance (Note 1)	TBD	°C/W
P_D	Power Dissipation in Still Air at 85°C	TBD	mW
MSL	Moisture Sensitivity	Level 1	
F_R	Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	> 2000 > 200 N/A	V
$I_{Latchup}$	Latchup Performance Above V_{CC} and Below GND at 125°C (Note 5)	± 500	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2-ounce copper trace with no air flow.
2. Tested to EIA/JESD22-A114-A.
3. Tested to EIA/JESD22-A115-A.
4. Tested to JESD22-C101-A.
5. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Power DC Supply Voltage Operating Data Retention Only	1.65 1.5	5.5 5.5	V
V_{IN}	Digital Input Voltage (Note 6)	0	5.5	V
V_{OUT}	Output Voltage	0	V_{CC}	V
T_A	Operating Free-Air Temperature	-55	+125	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate $V_{CC} = 1.8 V \pm 0.15 V$ $V_{CC} = 2.5 V \pm 0.2 V$ $V_{CC} = 3.3 V \pm 0.3 V$ $V_{CC} = 5.0 V \pm 0.5 V$	0 0 0 0	20 20 10 5	ns/V

6. Unused inputs may not be left open. All inputs must be tied to a high- or low-logic input voltage level.

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DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V _{CC} (V)	T _A = 25°C			T _A ≤ 85°C		T _A = -55°C to +125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V _{IH}	High-Level Input Voltage		1.65 2.3 to 5.5	0.75 x V _{CC} 0.7 x V _{CC}			0.75 x V _{CC} 0.7 x V _{CC}		0.75 x V _{CC} 0.7 x V _{CC}		V
V _{IL}	Low-Level Input Voltage		1.65 2.3 to 5.5			0.25 x V _{CC} 0.3 x V _{CC}		0.25 x V _{CC} 0.3 x V _{CC}		0.25 x V _{CC} 0.3 x V _{CC}	V
V _{OH}	High-Level Output Voltage	V _{IN} = V _{IH} or V _{IL} , I _{OH} = -100 μA	1.65 to 5.5	V _{CC} - 0.1	V _{CC}		V _{CC} - 0.1		V _{CC} - 0.1		V
		V _{IN} = V _{IH} or V _{IL} I _{OH} = -4 mA	1.65	1.29	1.5		1.29		1.29		
		I _{OH} = -8 mA	2.3	1.9	2.1		1.9		1.9		
		I _{OH} = -12 mA	2.7	2.2	2.4		2.2		2.2		
		I _{OH} = -16 mA	3.0	2.4	2.7		2.4		2.4		
		I _{OH} = -24 mA	3.0	2.3	2.5		2.3		2.3		
I _{OH} = -32 mA	4.5	3.8	4.0		3.8		3.8				
V _{OL}	Low-Level Output Voltage	V _{IN} = V _{IH} or V _{IL} , I _{OL} = 100 μA	1.65 to 5.5			0.1		0.1		0.1	V
		V _{IN} = V _{IH} or V _{IL} I _{OL} = 4 mA	1.65		0.08	0.24		0.24		0.24	
		I _{OL} = 8 mA	2.3		0.20	0.3		0.3		0.3	
		I _{OL} = 12 mA	2.7		0.22	0.4		0.4		0.4	
		I _{OL} = 16 mA	3.0		0.28	0.4		0.4		0.4	
		I _{OL} = 24 mA	3.0		0.38	0.55		0.55		0.55	
I _{OL} = 32 mA	4.5		0.42	0.55		0.55		0.55			
I _{IN}	Input Leakage Current	0 ≤ V _{IN} ≤ 5.5 V	0 to 5.5			±0.1		±1.0		±1.0	μA
I _{OFF}	Power-Off Input Leakage Current	V _{IN} = 5.5 V	0			1.0		10		10	μA
I _{CC}	Quiescent Supply Current	0 ≤ V _{IN} ≤ 5.5 V	5.5			1.0		10		10	μA

AC ELECTRICAL CHARACTERISTICS t_R = t_F = 2.5 ns

Symbol	Parameter	V _{CC} (V)	Test Condition	T _A = 25°C			T _A ≤ 85°C		T _A = -55°C to +125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation Delay Input A to Output	1.65 to 1.95	R _L = 1 MΩ, C _L = 15 pF	2.0	5.7	10.5	2.0	11.0	TBD	TBD	ns
		2.3 to 2.7	R _L = 1 MΩ, C _L = 15 pF	1.2	3.2	5.3	1.2	5.7	TBD	TBD	
		3.0 to 3.6	R _L = 1 MΩ, C _L = 15 pF	0.8	2.4	3.7	0.8	4.0	TBD	TBD	
			R _L = 500 Ω, C _L = 50 pF	1.2	3.0	4.6	1.2	4.9	TBD	TBD	
4.5 to 5.5	R _L = 1 MΩ, C _L = 15 pF	0.5	1.9	2.9	0.5	3.2	TBD	TBD			
	R _L = 500 Ω, C _L = 50 pF	0.8	2.4	3.6	0.8	3.9	TBD	TBD			
C _{IN}	Input Capacitance	5.5	V _{IN} = 0 V or V _{CC}		2.5						pF
C _{PD}	Power Dissipation Capacitance (Note 7)	3.3	10 MHz, V _{IN} = 0V or V _{CC}		9						pF
		5.5			11						

7. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}. C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

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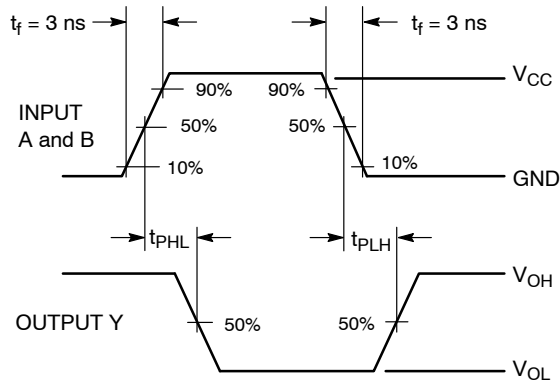
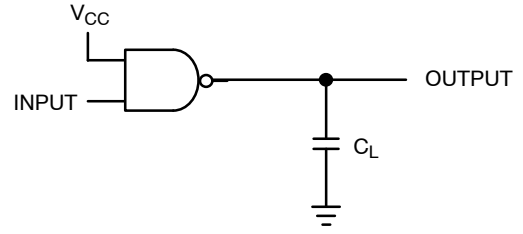


Figure 3. Switching Waveform



A 1-MHz square input wave is recommended for propagation delay tests.

Figure 4. Test Circuit

ORDERING INFORMATION

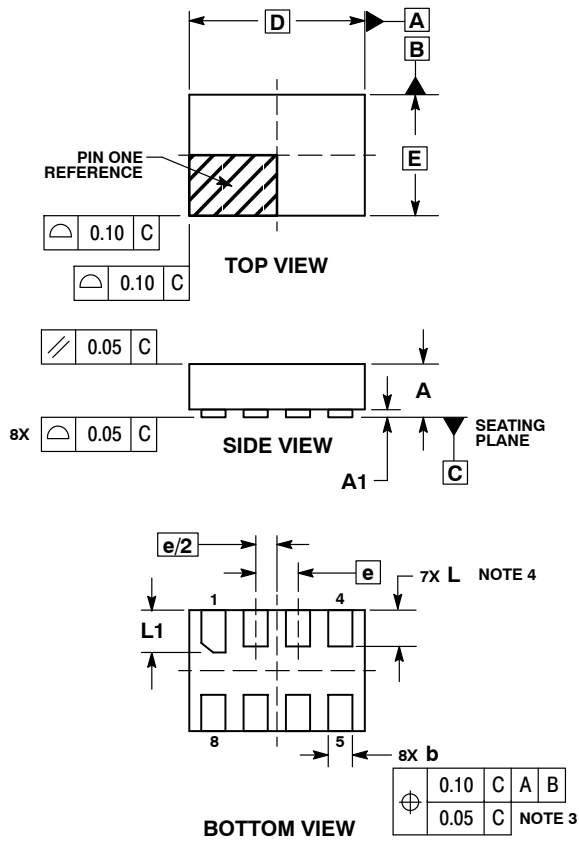
Device	Package	Shipping†
NLX2G00AMX1TCG	ULLGA8, 1.95 x 1.0, 0.5P (Pb-Free)	3000 / Tape & Reel
NLX2G00BMX1TCG	ULLGA8, 1.6 x 1.0, 0.4P (Pb-Free)	3000 / Tape & Reel
NLX2G00CMX1TCG	ULLGA8, 1.45 x 1.0, 0.35P (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NLX2G00

PACKAGE DIMENSIONS

ULLGA8 1.45x1.0, 0.35P
CASE 613AA-01
ISSUE A

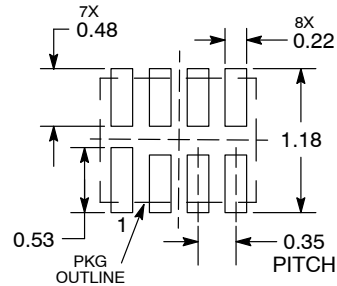


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
4. A MAXIMUM OF 0.05 PULL BACK OF THE PLATED TERMINAL FROM THE EDGE OF THE PACKAGE IS ALLOWED.

MILLIMETERS		
DIM	MIN	MAX
A	---	0.40
A1	0.00	0.05
b	0.15	0.25
D	1.45 BSC	
E	1.00 BSC	
e	0.35 BSC	
L	0.25	0.35
L1	0.30	0.40

**MOUNTING FOOTPRINT
SOLDERMASK DEFINED***



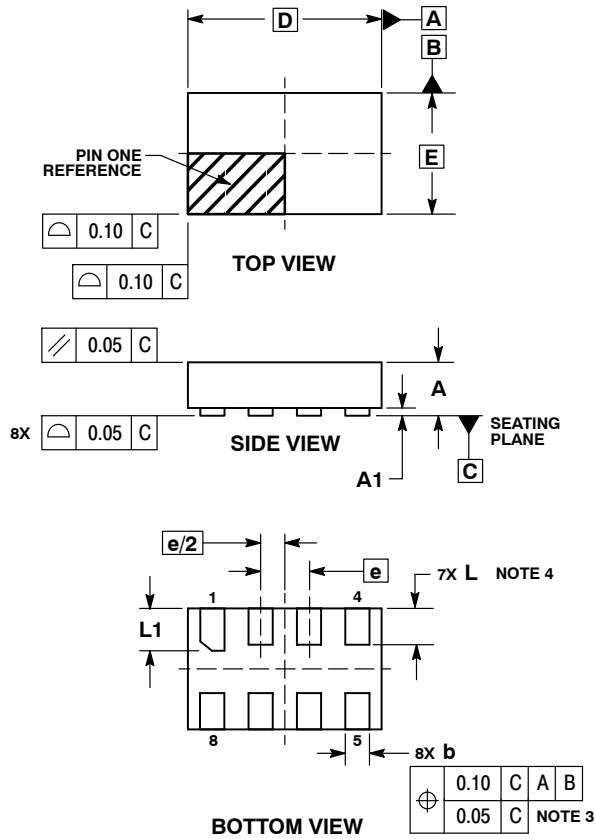
DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NLX2G00

PACKAGE DIMENSIONS

ULLGA8 1.6x1.0, 0.4P
CASE 613AB-01
ISSUE A

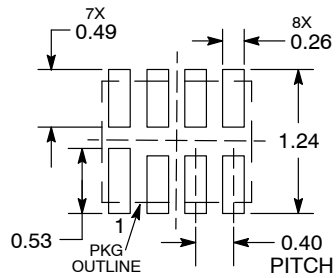


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4. A MAXIMUM OF 0.05 PULL BACK OF THE PLATED TERMINAL FROM THE EDGE OF THE PACKAGE IS ALLOWED.

MILLIMETERS		
DIM	MIN	MAX
A	---	0.40
A1	0.00	0.05
b	0.15	0.25
D	1.60 BSC	
E	1.00 BSC	
e	0.40 BSC	
L	0.25	0.35
L1	0.30	0.40

**MOUNTING FOOTPRINT
SOLDERMASK DEFINED***



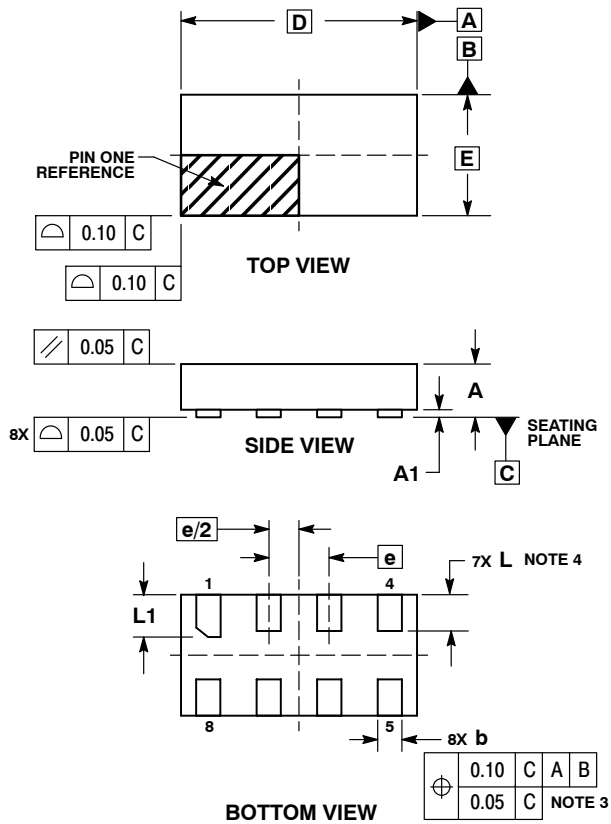
DIMENSIONS: MILLIMETERS

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PACKAGE DIMENSIONS

ULLGA8 1.95x1.0, 0.5P
CASE 613AC-01
ISSUE A

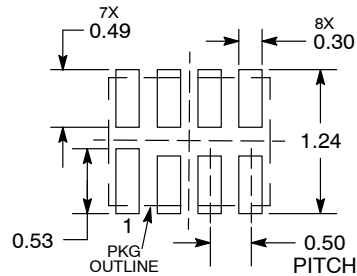


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MILLIMETERS		
DIM	MIN	MAX
A	---	0.40
A1	0.00	0.05
b	0.15	0.25
D	1.95 BSC	
E	1.00 BSC	
e	0.50 BSC	
L	0.25	0.35
L1	0.30	0.40

**MOUNTING FOOTPRINT
SOLDERMASK DEFINED***



DIMENSIONS: MILLIMETERS

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